IN THE SPECIFICATION

Please replace paragraph [0077] with the following paragraph:

[0077] **Figure 9** illustrates an embodiment of a clock recovery circuit 901 for use in an optical receiver. Some embodiments of clock recovery circuit 901 comprise a delay locked loop (DLL) 911 and a phase interpolator 932 to generate an aligned clock signal from the reference clock signal received from an optical channel. In operation, the reference clock signal, CLK, is input to DLL 911. DLL 911 may generate multiple equally-delayed differential signals. These multiple equally-delayed differential signals may be buffered by clock buffering circuitry 920 for input to phase interpolator 932. Clock buffering circuitry 920 comprises controlled delay elements 921-924. The delays of controlled delay elements 921-924 along with controlled delay element 910 may be adjusted by DLL 911 control voltage(s). The phase interpolator 932 aligns the edges of the aligned clock signal, CLK_{OUT}, with a data stream center in a much higher resolution.